

What is claimed is:

- 1 1. An inverting delay component, comprising:
 - 2 an inverting portion having an input terminal for receiving an input signal, a
 - 3 complementary input terminal for receiving a complement of the input
 - 4 signal, an output terminal for providing an output signal, and a
 - 5 complementary output terminal for providing a complement of the output
 - 6 signal, the inverting portion performing an inverting function such that the
 - 7 output signal is an inverted version of the complement of the input signal,
 - 8 and the complement of the output signal is an inverted version of the input
 - 9 signal; and
- 10 a delay control portion, comprising:
 - 11 a first current source having a first impedance, the first current source
 - 12 coupled to the complementary output terminal and also coupled to
 - 13 receive a control signal;
 - 14 a first resistive element coupled to the first current source, the first
 - 15 resistive element causing the first current source to exhibit an
 - 16 output impedance which is much larger than the first impedance;
 - 17 a second current source having a second impedance, the second current
 - 18 source coupled to the output terminal and also coupled to receive
 - 19 the control signal; and
- 20 a second resistive element coupled to the second current source, the
- 21 second resistive element causing the second current source to

exhibit an output impedance which is much larger than the second
impedance.

1 2. The component of claim 1, wherein the first current source comprises a
2 first transistor having a drain terminal coupled to the complementary output terminal, a
3 gate terminal coupled to receive the control signal, and a source terminal coupled to the
4 first resistive element.

1 3. The component of claim 2, wherein the second current source comprises a
2 second transistor having a drain terminal coupled to the output terminal, a gate terminal
3 coupled to receive the control signal, and a source terminal coupled to the second
4 resistive element.

1 4. The component of claim 3, wherein the first resistive element comprises a
2 first resistor and the second resistive element comprises a second resistor.

1 5. The component of claim 3, wherein the first resistive element comprises a
2 third transistor biased to behave like a resistor, and the second resistive element
3 comprises a forth transistor biased to behave like a resistor.

1 6. The component of claim 1, wherein the inverting portion comprises:

2 a first transistor having a gate terminal coupled to the input terminal, a drain
3 terminal coupled to the complementary output terminal, and a source terminal coupled to
4 a first node;
5 a second transistor having a gate terminal coupled to the complementary input
6 terminal, a drain terminal coupled to the output terminal, and a source terminal coupled to
7 the first node;
8 a third transistor having a gate terminal coupled to the output terminal, a drain
9 terminal coupled to the complementary output terminal, and a source terminal coupled to
10 the first node; and
11 a fourth transistor having a gate terminal coupled to the complementary output
12 terminal, a drain terminal coupled to the output terminal, and a source terminal coupled to
13 the first node.

1 7. The component of claim 6, wherein the inverting portion further
2 comprises:
3 a fifth transistor having a gate terminal coupled to the complementary output
4 terminal, a drain terminal coupled to the complementary output terminal, and a source
5 terminal coupled to the first node; and
6 a sixth transistor having a gate terminal coupled to the output terminal, a drain
7 terminal coupled to the output terminal, and a source terminal coupled to the first node.

1 8. The component of claim 7, wherein the first current source comprises a
2 seventh transistor having a drain terminal coupled to the complementary output terminal,

3 a gate terminal coupled to receive the control signal, and a source terminal coupled to the
4 first resistive element, and wherein the second current source comprises an eighth
5 transistor having a drain terminal coupled to the output terminal, a gate terminal coupled
6 to receive the control signal, and a source terminal coupled to the second resistive
7 element.

1 9. The component of claim 8, wherein the first resistive element comprises a
2 first resistor, and wherein the second resistive element comprises a second resistor.

1 10. The component of claim 8, wherein the first resistive element comprises a
2 ninth transistor biased to behave like a resistor, and the second resistive element
3 comprises a tenth transistor biased to behave like a resistor.

1 11. An oscillator, comprising:
2 an n number of inverting delay components coupled in series to form a closed
3 loop circuit, where n is an odd integer greater than one, each inverting delay component
4 comprising:
5 an inverting portion having an input terminal for receiving an input signal,
6 a complementary input terminal for receiving a complement of the
7 input signal, an output terminal for providing an output signal, and
8 a complementary output terminal for providing a complement of
9 the output signal, the inverting portion performing an inverting
10 function such that the output signal is an inverted version of the

11 complement of the input signal, and the complement of the output
12 signal is an inverted version of the input signal; and
13 a delay control portion, comprising:
14 a first current source having a first impedance, the first current
15 source coupled to the complementary output terminal and
16 also coupled to receive a control signal;
17 a first resistive element coupled to the first current source, the first
18 resistive element causing the first current source to exhibit
19 an output impedance which is much larger than the first
20 impedance;
21 a second current source having a second impedance, the second
22 current source coupled to the output terminal and also
23 coupled to receive the control signal; and
24 a second resistive element coupled to the second current source,
25 the second resistive element causing the second current
26 source to exhibit an output impedance which is much larger
27 than the second impedance;
28 wherein the input terminal and the complementary input terminal are
29 coupled to a complementary output terminal and an output
30 terminal, respectively, of a preceding inverting delay component,
31 and

32 wherein the output terminal and the complementary output terminal are
33 coupled to a complementary input terminal and an input terminal,
34 respectively, of a succeeding inverting delay element.

1 12. The oscillator of claim 11, wherein the first current source comprises a
2 first transistor having a drain terminal coupled to the complementary output terminal, a
3 gate terminal coupled to receive the control signal, and a source terminal coupled to the
4 first resistive element.

1 13. The oscillator of claim 12, wherein the second current source comprises a
2 second transistor having a drain terminal coupled to the output terminal, a gate terminal
3 coupled to receive the control signal, and a source terminal coupled to the second
4 resistive element.

1 14. The oscillator of claim 13, wherein the first resistive element comprises a
2 first resistor and the second resistive element comprises a second resistor.

1 15. The oscillator of claim 13, wherein the first resistive element comprises a
2 third transistor biased to behave like a resistor, and the second resistive element
3 comprises a forth transistor biased to behave like a resistor.

1 16. The oscillator of claim 11, wherein the inverting portion comprises:

2 a first transistor having a gate terminal coupled to the input terminal, a drain
3 terminal coupled to the complementary output terminal, and a source terminal coupled to
4 a first node;
5 a second transistor having a gate terminal coupled to the complementary input
6 terminal, a drain terminal coupled to the output terminal, and a source terminal coupled to
7 the first node;
8 a third transistor having a gate terminal coupled to the output terminal, a drain
9 terminal coupled to the complementary output terminal, and a source terminal coupled to
10 the first node; and
11 a fourth transistor having a gate terminal coupled to the complementary output
12 terminal, a drain terminal coupled to the output terminal, and a source terminal coupled to
13 the first node.

1 17. The oscillator of claim 16, wherein the inverting portion further
2 comprises:
3 a fifth transistor having a gate terminal coupled to the complementary output
4 terminal, a drain terminal coupled to the complementary output terminal, and a source
5 terminal coupled to the first node; and
6 a sixth transistor having a gate terminal coupled to the output terminal, a drain
7 terminal coupled to the output terminal, and a source terminal coupled to the first node.

1 18. The oscillator of claim 17, wherein the first current source comprises a
2 seventh transistor having a drain terminal coupled to the complementary output terminal,

3 a gate terminal coupled to receive the control signal, and a source terminal coupled to the
4 first resistive element, and wherein the second current source comprises an eighth
5 transistor having a drain terminal coupled to the output terminal, a gate terminal coupled
6 to receive the control signal, and a source terminal coupled to the second resistive
7 element.

1 19. The oscillator of claim 18, wherein the first resistive element comprises a
2 first resistor, and wherein the second resistive element comprises a second resistor.

1 20. The oscillator of claim 18, wherein the first resistive element comprises a
2 ninth transistor biased to behave like a resistor, and the second resistive element
3 comprises a tenth transistor biased to behave like a resistor.